In accordance with the guidelines and waived provisions of 37 C.F.R. 1.121 promulgated in the USPTO announcement of January 31, 2003, please make the following amendments.

IN THE CLAIMS:

Please amend the claims as follows.

1.-27. (Canceled)

28. (Currently Amended) A semiconductor device including a CMOS circuit formed by an n-channel TFT and a p-channel TFT, ~~characterized in that:~~

~~the CMOS circuit has a structure that~~ wherein an active layer of the n-channel TFT is sandwiched by a first wiring line and a second wiring line through insulating layers ~~in only the n-channel TFT~~,

wherein the active layer includes a low concentration impurity region that is in contact with a channel formation region; and

wherein the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line.

29. (Currently Amended) A semiconductor device according to claim 28, ~~[characterized in that]~~ wherein the first wiring line is electrically connected with the second wiring line.

30. (Currently Amended) A semiconductor device including a CMOS circuit formed by an n-channel TFT and a p-channel TFT, ~~characterized in that:~~

~~the CMOS circuit has a structure that~~ wherein an active layer of the n-channel TFT is sandwiched by a first wiring line and a second wiring line through insulating layers ~~in only the n-channel TFT~~; and

wherein the second wiring line has a portion ~~of structure laminated with~~ being a laminate of a first conductive layer and a ~~second~~ third conductive layer, and a portion ~~of structure wrapped a third conductive layer with~~ being a laminate of the first conductive

layer ~~and~~ , ~~the~~ a second conductive layer and the third conductive layer.

31. (Currently Amended) A semiconductor device according to claim 30, ~~characterized in that~~ wherein the third conductive layer has a lower resistance value than the first conductive layer ~~or~~ and the second conductive layer.

32. (Currently Amended) A semiconductor device according to claim 30, ~~characterized in that~~ wherein at least one of the first wiring line ~~or~~ and the second wiring line ~~is appropriately a conductive film mainly containing~~ contains an element selected from the group consisting of tantalum (Ta), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si)~~, or an alloy film or silicide film containing the above elements in combination~~.

D1 Cont.

33. (Currently Amended) A semiconductor device according to claim 30, ~~characterized in that~~ wherein the third conductive layer ~~is appropriately a conductive film~~ mainly ~~containing~~ contains one of aluminum (Al) ~~or~~ and copper (Cu).

34. (Currently Amended) A semiconductor device having a pixel matrix circuit that includes a pixel TFT and a storage capacitor formed ~~in~~ by an n-channel TFT, ~~characterized in that~~

wherein the pixel TFT has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through insulating layers,

wherein the active layer includes a low concentration impurity region that is in contact with a channel formation region; and

wherein the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line.

35. (Currently Amended) A semiconductor device according to claim 34, ~~characterized in that~~ wherein the first wiring line is kept at one of a ground electric potential ~~or at~~ and a source power supply electric potential.

36. (Currently Amended) A semiconductor device according to claim 34, ~~characterized in that~~ wherein the first wiring line is kept at a floating electric potential.

37. (Currently Amended) A semiconductor device having a pixel matrix circuit that includes a pixel TFT and a storage capacitor formed ~~in~~ by an n-channel TFT, ~~characterized in that~~

wherein the pixel TFT has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through insulating layers, and

wherein the second wiring line has a portion ~~of structure laminated with~~ being a laminate of a first conductive layer and a ~~second~~ third conductive layer, and a portion ~~of structure wrapped a third conductive layer with~~ being a laminate of the first conductive layer ~~and~~ , ~~the~~ a second conductive layer and the third conductive layer.

D1 Cont.

38. (Currently Amended) A semiconductor device according to claim 37, ~~characterized in that~~ wherein the third conductive layer has a lower resistance value than the first conductive layer ~~or~~ and the second conductive layer.

39. (Currently Amended) A semiconductor device according to claim 37, ~~characterized in that~~ wherein at least one of the first wiring line ~~or~~ and the second wiring line [is appropriately a conductive film mainly containing] contains an element selected from the group consisting of tantalum (Ta), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si)~~, or an alloy film or silicide film containing the above elements in combination~~.

40. (Currently Amended) A semiconductor device according to claim 37, ~~characterized in that~~ wherein the third conductive layer ~~is appropriately a conductive film~~ mainly ~~containing~~ contains one of aluminum (Al) ~~or~~ and copper (Cu).

41. (Currently Amended) A semiconductor device having a pixel matrix

circuit and a driver circuit that are formed on a same substrate, ~~characterized in that~~

wherein each of a pixel TFT included in the pixel matrix circuit and an n-channel TFT included in the driver circuit ~~have~~ has a structure that each of ~~an~~ active ~~layer~~ layers is sandwiched by each of ~~a~~ first wiring ~~line~~ lines and each of ~~a~~ second wiring ~~line~~ lines through each of insulating layers; and

wherein the first wiring line ~~connected to~~ of the pixel TFT is kept at one of a fixed electric potential ~~or~~ and a floating electric potential, and the first wiring line ~~connected to~~ of the n-channel TFT included in the driver circuit is kept at ~~a~~ the same level of electric potential as the second wiring line ~~connected to~~ of the n-channel TFT included in the driver circuit.

42. (Canceled)

43. (Canceled)

44. (Previously Canceled)

45. (Currently Amended) A semiconductor device according to claim 41, ~~characterized in that~~ wherein each of the first wiring line or each of the second wiring line ~~is appropriately a conductive film mainly containing~~ contains an element selected from the group consisting of tantalum (Ta), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si)~~, or an alloy film or silicide film containing the above elements in combination~~.

46. (Previously Canceled)

47. (Currently Amended) ~~A~~ semiconductor device according to any one of claims 28 to ~~46~~ 43 and 45, wherein the semiconductor device is one of an active matrix liquid crystal display ~~or~~ and an active matrix EL display.

48. (Currently Amended) A semiconductor device according to any one of claims 28 to ~~46~~ 43 and 45, wherein the semiconductor device is one selected from the group consisting of a video camera, a digital camera, a projector, a projection TV, a goggle type display, an automobile navigation system, a personal computer, ~~or~~ and a portable information terminal.

49.-54. (Previously Canceled)

55. (New) A semiconductor device having a pixel matrix circuit and a driver circuit that are formed on a same substrate,

wherein each of a pixel TFT included in the pixel matrix circuit and an n-channel TFT included in the driver circuit has a structure that each of active layers is sandwiched by each of first wiring lines and each of second wiring lines through each of insulating layers;

wherein each of the active layers includes a low concentration impurity region that is in contact with each of channel formation regions;

wherein each of the low concentration impurity regions is formed to overlap each of the first wiring lines and not to overlap each of the second wiring lines; and

wherein the first wiring line of the pixel TFT is kept at one of a fixed electric potential and a floating electric potential, and the first wiring line of the n-channel TFT included in the driver circuit is kept at the same level of electric potential as the second wiring line of the n-channel TFT included in the driver circuit.

56. (New) A semiconductor device according to claim 55, the semiconductor device is one of an active matrix liquid crystal display and an active matrix EL display.

57. (New) A semiconductor device according to claim 55, the semiconductor device is one selected from the group consisting of a video camera, a digital camera, a projector, a projection TV, a goggle type display, an automobile navigation system, a personal computer, and a portable information terminal.

58. (New) A semiconductor device having a pixel matrix circuit and a driver circuit that are formed on a same substrate,

wherein each of a pixel TFT included in the pixel matrix circuit and an n-channel TFT included in the driver circuit has a structure that each of active layers is sandwiched by each of first wiring lines and each of second wiring lines through each of insulating layers;

wherein at least one of the second wiring lines has a portion being a laminate of a first conductive layer and a third conductive layer, and a portion being a laminate of the first conductive layer, a second conductive layer and the third conductive layer, and

wherein the first wiring line of the pixel TFT is kept at one of a fixed electric potential and a floating electric potential, and the first wiring line of the n-channel TFT included in the driver circuit is kept at the same level of electric potential as the second wiring line of the n-channel TFT included in the driver circuit.

D1 Cont.

59. (New) A semiconductor device according to claim 58, wherein the third conductive layer has a lower resistance value than the first conductive layer and the second conductive layer.

60. (New) A semiconductor device according to claim 58, wherein at least one of the first wiring line and the second wiring line contains an element selected from the group consisting of tantalum (Ta), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si).

61. (New) A semiconductor device according to claim 58, wherein the third conductive layer mainly contains one of aluminum (Al) and copper (Cu).

62. (New) A semiconductor device according to claim 58, wherein the semiconductor device is one of an active matrix liquid crystal display and an active matrix EL display.

63. (New) A semiconductor device according to claim 58, wherein the semiconductor device is one selected from the group consisting of a video camera, a digital camera, a projector, a projection TV, a goggle type display, an automobile navigation system, a personal computer, and a portable information terminal.